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Wang, M.; Jin Yuan Wu;  
[Real Time Conference, 2005. 14th IEEE-NPSS](#)  
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- ☐ **4. Integrated upstream parasitic event building architecture for BTeV level 1 system**  
Jinyuan Wu; Wang, M.; Gottschalk, E.; Christian, D.; Li, X.; Shi, Z.; Pavlicek, V  
[Real Time Conference, 2005. 14th IEEE-NPSS](#)  
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Wang, M.; Suzuki, K.; Dai, W.; Sakai, A.; Watanabe, K.;  
[Solid State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th 18-20 Sept. 2001](#) Page(s):385 - 388  
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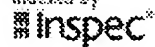
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L8	6	simulat\$3 same particle same distribution and ray and voxel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/04/18 14:38
L9	78	emulat\$4 same FPGA same network	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/04/18 14:57

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L11	122	emulat\$4 same FPGA and network adj interface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/04/18 14:57
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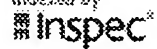
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